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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/192,164	11/13/98	SMITH S	014823-116

021839 LM02/0203
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EXAMINER	
GREENE, J	
ART UNIT	**PAPER NUMBER**
2784	5

DATE MAILED: 02/03/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/192,164	Shawn Smith, et al.
Examiner	**Group Art Unit**
Jason Greene	2784

☒ Responsive to communication(s) filed on *Nov 13, 1998*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-9* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-9* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

— SEE OFFICE ACTION ON THE FOLLOWING PAGES —

DETAILED ACTION

1. Claims 1-9 are presented for examination.

Claim Rejections - 35 USC § 112

2. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The phrase "substantially continuously" in the 3rd line of the second claim is indefinite.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

4. Claims 1 and 4-6 are rejected under 35 U.S.C. 102(b) as being anticipated by the article, "High Yield Multichip Modules Based on Minimal IC Pretest" by Burdick et al.(Burdick, W.; Daum, W.; Test Conference, 1994. Proceedings., International, 1994, pages 30-40).

5. As to claim 1, Burdick et al. teaches the invention as claimed including a method of automated defect localization in the testing of semiconductor integrated circuits, comprising the steps of:

a. testing the integrated circuits to obtain generalized failure data("High Yield Multichip Modules Based on Minimal IC Pretest"; page 32, section 5 - Classification of ICs and Pretest Methods, 4th paragraph);

b. inputting the generalized failure data to a circuit analysis tool("High Yield Multichip Modules Based on Minimal IC Pretest"; page 32, section 5 - Classification of ICs and Pretest Methods, 4th paragraph);

c. obtaining from the circuit analysis first localized probable defect data("High Yield Multichip Modules Based on Minimal IC Pretest"; page 32, section 5 - Classification of ICs and Pretest Methods, 4th paragraph; page 33, left column, 2nd paragraph);

d. performing in-line inspection of the integrated circuits to obtain second localized probable defect data("High Yield Multichip Modules Based on Minimal IC Pretest"; page 32,

section 5 - Classification of ICs and Pretest Methods, 6th paragraph; page 33, left column, first paragraph); and

e. correlating the first and second localized probable defect data("High Yield Multichip Modules Based on Minimal IC Pretest"; page 33, left column, first paragraph).

6. As to claim 4, Burdick et al. teaches the invention as claimed including a method of automated defect localization in the testing of semiconductor integrated circuits, wherein the integrated circuits are logic circuits having built-in-self-test capabilities.

While Burdick et al. didn't specifically teach using BISTed circuits, Burdick et al. did specifically teach that the process could be used for several types of circuits which commonly contain BIST elements("High Yield Multichip Modules Based on Minimal IC Pretest"; page 32, section 5 - Classification of ICs and Pretest Methods, 4th paragraph).

7. As to claim 5, Burdick et al. teaches the invention as claimed including a method of automated defect localization in the testing of semiconductor integrated circuits, wherein the generalized failure data is obtained using end-of-line testing of the integrated circuit("High Yield Multichip Modules Based on Minimal IC Pretest"; page 32, section 5 - Classification of ICs and Pretest Methods, 4th paragraph; page 33, left column, 2nd paragraph).

8. As to claim 6, teaches the invention as claimed including a method of automated defect localization in the testing of semiconductor integrated circuits, wherein the integrated circuits are tested in wafer form("High Yield Multichip Modules Based on Minimal IC Pretest"; page 32, section 5 - Classification of ICs and Pretest Methods, 2nd paragraph).

9. Claims 1-8 rejected under 35 U.S.C. 102(e) as being anticipated by Lindsay(Patent No. 5,720,031).

10. As to claim 1, Lindsay teaches the invention as claimed including a method of automated defect localization in the testing of semiconductor integrated circuits, comprising the steps of:

a. testing the integrated circuits to obtain generalized failure data(col 5, lines 62-67 to col 6, lines 1-2);

b. inputting the generalized failure data to a circuit analysis tool(col 6, lines 12-18);

c. obtaining from the circuit analysis first localized probable defect data(col 6, lines 9-12);

d. performing in-line inspection of the integrated circuits to obtain second localized probable defect data(col 5, lines 45-48); and

e. correlating the first and second localized probable defect data(col 7, lines 2-7; col 9, lines 14-19).

11. As to claim 2, Lindsay teaches the invention as claimed including a method of automated defect localization in the testing of semiconductor integrated circuits, wherein the steps of inputting the generalized failure data to a circuit analysis tool and obtaining from the circuit analysis first localized probable defect data are performed substantially continuously using at least one programmed computer(col 7, lines 28-35).

12. As to claim 3, Lindsay teaches the invention as claimed including a method of automated defect localization in the testing of semiconductor integrated circuits, wherein correlating the first and second localized probable defect data comprises producing a visual overlay of the first and second localized probable defect data(see abstract; col 1, lines 56-67 to column 2, lines 1-14; col 7, lines 2-7; col 9, lines 14-19).

13. As to claim 4, Lindsay teaches the invention as claimed including a method of automated defect localization in the testing of semiconductor integrated circuits, wherein the integrated circuits are logic circuits having built-in-self-test capabilities.

While Lindsay did not specifically teach using BISTed circuits he does teach performing his testing apparatus on semiconductor memory devices, which commonly contain BIST elements.

14. As to claim 5, Lindsay teaches the invention as claimed including a method of automated defect localization in the testing of semiconductor integrated circuits, wherein the generalized failure data is obtained using end-of-line testing of the integrated circuit(col 5, lines 62-67 to col 6, lines 1-2).

15. As to claim 6, Lindsay teaches the invention as claimed including a method of automated defect localization in the testing of semiconductor integrated circuits, wherein the integrated circuits are tested in wafer form(col 5, lines 42-43).

16. As to claim 7, Lindsay teaches the invention as claimed including a method of automated defect localization in the testing of semiconductor integrated circuits, wherein obtaining from the circuit analysis first localized probable defect data comprises:

a. creating a database against which logic defect data is processed to obtain physical defect data(col 6, lines 9-12, lines 57-67 to col 7, lines 1-7); and

b. processing the logical defect data against the database to obtain physical defect data(col 6, lines 9-12, lines 57-67 to col 7, lines 1-7).

17. As to claim 8, Lindsay teaches the invention as claimed including a method of automated defect localization in the testing of semiconductor integrated circuits, wherein creating the

database comprises translating design information from a first format to a second format(col 6, lines 9-12, lines 57-67 to col 7, lines 1-7).

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 2, 3, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over "High Yield Multichip Modules Based on Minimal IC Pretest" by Burdick et al.(Burdick, W.; Daum, W.; Test Conference, 1994. Proceedings., International, 1994, pages 30-40) in view of Lindsay(Patent No. 5,720,031).

20. As to claim 2, Burdick et al. teaches the invention as substantially as claimed with the exception of specifically teaching the following step: a method of automated defect localization in the testing of semiconductor integrated circuits, wherein the steps of inputting the generalized failure data to a circuit analysis tool and obtaining from the circuit analysis first localized

probable defect data are performed substantially continuously using at least one programmed computer.

However, Lindsay teaches the above claimed feature(col 7, lines 28-35). Therefore it would have been obvious to one of ordinary skill in the art to combine the physical default mapping system of Lindsay into the system of pre testing wafers of Burdick et al as it would allow the system of Burdick et al. to perform its function tests and visual inspection tests even more effectively by showing the location of function test faults possibly caused by physical defects.

21. As to claim 3, Burdick et al. teaches the invention as substantially as claimed with the exception of specifically teaching the following step: a method of automated defect localization in the testing of semiconductor integrated circuits, wherein correlating the first and second localized probable defect data comprises producing a visual overlay of the first and second localized probable defect data.

However, Lindsay teaches the above claimed feature(see abstract; col 1, lines 56-67 to column 2, lines 1-14; col 7, lines 2-7; col 9, lines 14-19). Therefore it would have been obvious to one of ordinary skill in the art to combine the physical default mapping system of Lindsay into the system of pre testing wafers of Burdick et al as it would allow the system of Burdick et al. to perform its function tests and visual inspection tests even more effectively by showing the location of function test faults possibly caused by physical defects.

22. As to claim 7, Burdick et al. teaches the invention as substantially as claimed with the exception of specifically teaching the following step: a method of automated defect localization in the testing of semiconductor integrated circuits, wherein obtaining from the circuit analysis first localized probable defect data comprises:

a. creating a database against which logic defect data is processed to obtain physical defect data(col 6, lines 9-12, lines 57-67 to col 7, lines 1-7); and

b. processing the logical defect data against the database to obtain physical defect data.

However, Lindsay teaches the above claimed feature(col 6, lines 9-12, lines 57-67 to col 7, lines 1-7).Therefore it would have been obvious to one of ordinary skill in the art to combine the physical default mapping system of Lindsay into the system of pre testing wafers of Burdick et al as it would allow the system of Burdick et al. to perform its function tests and visual inspection tests even more effectively by showing the location of function test faults possibly caused by physical defects.

23. As to claim 8, Lindsay teaches the invention as claimed including a method of automated defect localization in the testing of semiconductor integrated circuits, wherein creating the database comprises translating design information from a first format to a second format(col 6, lines 9-12, lines 57-67 to col 7, lines 1-7).

24. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lindsay(Patent No. 5,720,031).

25. As to claim 9, Lindsay teaches the invention substantially as claimed including a system for testing semiconductor integrated circuits comprising:

a. a circuit analysis tool(col 6, lines 12-18); and

b. means for automatically:

i. applying to the circuit analysis tool generalized failure data(col 5, lines 62-67 to col 6, lines 1-2);

ii. obtaining from the circuit analysis tool localized probable defect data(col 6, lines 9-12);

iii. representing the localized probable defect data in a standard format(col 6, lines 57-67 to col 7, lines 1-7);

Lindsay teaches the invention as claimed with the exception of specifically teaching the following step:

iv. storing the localized probable defect data on a database server accessible to multiple client machines.

However, the storing of data in a standard format on a database sever accessible to multiple client servers is a feature that is well known and widely used in the art. It would have been an obvious design choice to one of ordinary skill in the art at the time the invention was

made to store defect data or a truth/fault table developed from performing testing a semiconductor device on a database server so that its information might be accessible by any number of testing stations thereby saving testing time and money.

26. Claim 9 rejected under 35 U.S.C. 103(a) as being unpatentable over "High Yield Multichip Modules Based on Minimal IC Pretest" by Burdick et al.(Burdick, W.; Daum, W.; Test Conference, 1994. Proceedings., International, 1994, pages 30-40).

27. As to claim 9, Burdick et al. teaches the invention substantially as claimed including a system for testing semiconductor integrated circuits comprising:

a. a circuit analysis tool("High Yield Multichip Modules Based on Minimal IC Pretest"; page 32, section 5 - Classification of ICs and Pretest Methods, 3rd paragraph); and

b. means for automatically:

i. applying to the circuit analysis tool generalized failure data("High Yield Multichip Modules Based on Minimal IC Pretest"; page 32, section 5 - Classification of ICs and Pretest Methods, 4th paragraph);

ii. obtaining from the circuit analysis tool localized probable defect data("High Yield Multichip Modules Based on Minimal IC Pretest"; page 32, section 5 - Classification of ICs and Pretest Methods, 4th paragraph; page 33, left column, 2nd paragraph);

iii. representing the localized probable defect data in a standard format("High Yield Multichip Modules Based on Minimal IC Pretest"; page 33, right column, 1st paragraph, lines 5-7);

Burdick et al. teaches the invention as claimed with the exception of specifically teaching the following step:

iv. storing the localized probable defect data on a database server accessible to multiple client machines.

However, the storing of data in a standard format on a database sever accessible to multiple client servers is a feature that is well known and widely used in the art. It would have been an obvious design choice to one of ordinary skill in the art at the time the invention was made to store defect data or a truth/fault table developed from performing testing a semiconductor device on a database server so that its information might be accessible by any number of testing stations thereby saving testing time and money.

Conclusion

28. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 308-9051, (for formal communications intended for entry)

Or:

(703) 305-9724 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Greene whose telephone number is (703) 305-0080. The examiner can normally be reached on Tuesday to Friday from 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady, can be reached on (703) 305-9595.
Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Jason Greene
Examiner J.G.
Art Unit 2784

J.G.
January 20, 2000

ALBERT DE CADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2700